An Interference Tolerant RF Frontend With Capacitive Feedback for Channel Filtering

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***Abstract*—In this letter, a reconfigurable RF frontend with 4-path passive mixer is presented. Compared with the conventional method of using passive mixer at LNA output only, this design has further transferred the tunable impedance characteristic of passive mixer to the LNA input with capacitive feedback to achieve reconfigurable impedance matching at target frequency. Furthermore, the negative feedback is also able to free the conventional common base amplifier from 50 Ω impedance matching requirement to achieve better noise figure. The design was implemented with 0.18 μm SiGe BiCMOS technology. Measurement results showed a lowest noise figure of 4.6 dB from 0.6 to 1.1 GHz and an in-band IIP3 of −11 dBm, an out-band IIP3 of +3 dBm respectively.**

***Index Terms*—Capacitive feedback, passive mixer, receiver, reconfigurable frontend.**

I. Introduction

With the thriving of wireless technology, various new communication standards are emerging. A reconfigurable RF receiver frontend, in a software defined radio (SDR), will be able to selectively pick up signal over a wide bandwidth. One of the common issues with SDR is out-of-band interference. Recent academic research has focused on using passive mixer to address this issue. A mixer-first approach was demonstrated with excellent linearity at the cost of poor noise figure [1]. Others have proposed using passive mixer with a noise-cancelling LNA to achieve very low noise figure [2] using two paths of down-conversion which involves higher hardware complexity. In addition, precise gain and phase matching are required between paths which need extra calibration. In this design, we propose a reconfigurable receiver architecture that uses only one down-conversion path. The proposed LNA comes with a capacitive feedback that transfers the baseband filter profile to the input of the LNA to attenuate out-of-band interferers. The feedback also provides required input impedance only at the target frequency bands such that the out-of-band interferers cannot be delivered to the receiver input. Furthermore, the common-base (CB) amplifier with capacitive feedback allows independent optimization for noise and power matching, leading to a higher transconductance than that required by input matching to achieve lower noise figure.

Manuscript received February 4, 2016; revised April 28, 2016; accepted June 7, 2016. Date of publication August 16, 2016; date of current version September 1, 2016.

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Digital Object Identifier 10.1109/LMWC.2016.2597192

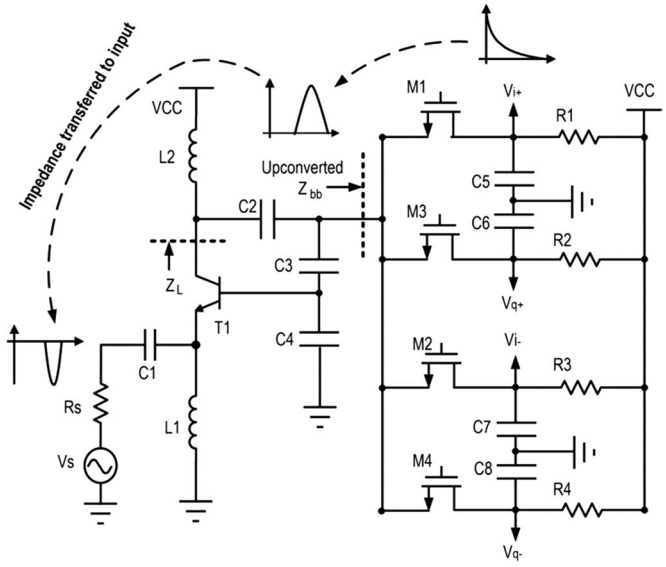

Fig. 1. Proposed receiver frontend and capacitive feedback.

This letter proposes a low noise frontend structure with tunable narrowband filtering and input matching. Section II will describe the proposed architecture with matching and gain analysis. Implementation details and measurement results will be shown in Section III.

II. Proposed Architecture

Owing to the good linearity and out-of-band interference robustness, passive mixer has been the focus of academic research recently as the most promising solution for highly flexible SDR frontend. In our proposed structure, the channel filtering profile of passive mixer is further transferred to the input of the receiver. Thus it can relax the requirement on LNA linearity while achieving a relatively low noise figure. As shown in Fig. 1, a common base amplifier acts as the first stage LNA. Bipolar transistor was used instead of MOSFET for better g_m efficiency as an advantage of BiCMOS technology. An integrated inductor was attached to T1's collector as a DC current feed. Output signal current from LNA was passed to a four-phase passive mixer. Due to the bandpass characteristic of passive mixer, only the voltage signals around LO frequency are developed at LNA output. The capacitor network consisting of C3 and C4 feeds this voltage signal back to T1's base, making the input impedance matched at the LO frequency only, thus the power from large out-of-band interferers will be reflected at the input of the receiver.

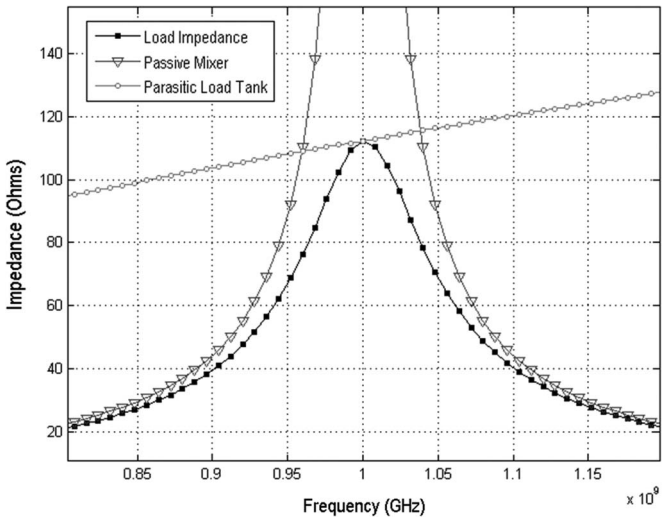

Fig. 2. Simulated LNA load impedance in which the peak load impedance is limited by the tank inductance while the floor is determined by the passive mixer.

A. Selective Gain Profile

In this section, we will analyze the selective gain (S21) profile of the LNA. Assuming the LNA load impedance to be Z_L as shown in Fig. 1, LNA voltage gain with the capacitive feedback can be shown to be

$$G = \frac{1}{A_V + \frac{R_S}{Z_L}} \tag{1}$$

where the feedback gain A_v is defined as the capacitance ratio

$$A_V = \frac{C3}{C3 + C4}. \tag{2}$$

The gain G is irrelevant to T1's g_m since it is assumed to be much larger than the source conductance (20 mS) in a conventional common-base amplifier and the gain is mainly determined by the resistance ratio. Furthermore, the LNA load impedance can be shown to be consisting of the parasitic load tank impedance and the baseband impedance upconverted by the passive mixer [2]

$$\begin{aligned} Z_L &= Z_{\text{tank,fold}}(w) \| Z_{\text{MX}}(w) \\ &= \frac{1}{\sum_{k=-\infty}^{+\infty} \frac{1}{(4k+1)^2 Z_{\text{tank}}(w+4kw_{\text{LO}})}} \left\| \frac{2}{\pi^2} \right. \\ &\quad \times (Z_{\text{BB}}(w - w_{\text{LO}}) + \text{Ron}) \\ &\approx Z_{\text{tank}}(w) \left\| \frac{2}{\pi^2} (Z_{\text{BB}}(w - w_{\text{LO}}) + \text{Ron}) \right. \end{aligned} \tag{3}$$

where

$$Z_{\text{tank}}(w) = \frac{1}{sC + \frac{1}{sL} + \frac{Av}{R_S + \frac{1}{g_m}}}.$$

In the above equation, higher orders of load impedance were ignored for simplicity. As shown in Fig. 2, the in-band load impedance is limited by the parasitic load tank (mainly the DC feed inductor L2). Since both inductor L1 and L2 served as DC current path only, they are chosen to be relatively large to avoid loading on the RF circuits: an integrated inductor of 22 nH was used for L1 and an off-chip inductor of 28 nH was chosen for L2. For out-band frequencies, the load impedance dropped to the switch resistance R_{on} ($\sim$20 Ω) of passive mixer. By taking these two values into (3), we can get a gain difference of about 14 dB which is close to the measurement result.

B. Input Matching

In our proposed structure, the input stage consists of a common base LNA with a feedback loop of C3 and C4 which was first proposed for reconfigurable receiver design [3]. With the negative feedback, the impedance characteristic at LNA output can be transferred to the LNA input as well

$$\text{Zin} = \frac{1}{g_m} + Av \cdot Z_L. \tag{4}$$

In this way the common base amplifier is no longer tied to a fixed g_m of 20 mS for input impedance matching which limits the lowest noise figure of common base amplifier to 3 dB. In fact, the g_m can be much higher for better noise figure. In the original design [3], the LNA load consists of an LC tank with a fixed resonant frequency. By attaching passive mixer as the load instead, we are essentially using a RF tank with tunable center frequency. Through tuning g_m and A_v, we can ensure that the LNA is matched to 50 Ω source resistance at target band only while presenting almost short impedance $(1/g_m)$ for out-band blockers.

C. Simplified Noise Analysis

For simplicity, the noise factor of the proposed receiver frontend can be approximated to the first order as

$$F \approx 1 + \frac{r_b}{R_s} + \frac{g_m R_s}{2\beta_0} + \frac{g_m R_s}{2\beta^2} + \frac{1}{2 g_m R_s} + \frac{R_{\text{on}} R_s}{Z_L^2} \tag{5}$$

where r_b, g_m, and R_{on} represents input transistor T1's base resistance, T1's trans-conductance and R_{on} represents the switch on resistance. The first few term comes from T1's base thermal noise, base shot noise and collector shot noise while the last term comes from the thermal noise of switch on resistance. It can be seen from this equation that higher g_m gives a lower noise contribution from LNA. By taking $dF/dR_s = 0$, we can calculate the optimum g_m for noise matching as

$$R_S^{\text{opt}} \approx \sqrt{\left(r_b + \frac{1}{2g_m}\right) \Big/ \left(\frac{g_m}{2\beta_0} + \frac{g_m}{2\beta^2} + \frac{R_{\text{on}}}{Z_L^2}\right)}. \tag{6}$$

For optimal noise matching at 50 Ω, the g_m calculated from (6) is much larger than that for power matching in a conventional CB LNA without feedback. With the capacitive feedback, we can now apply (4) and (6) to implement power matching and noise matching independently.

Steady-state simulation showed that the passive mixer is the major source of noise. Due to the switching behavior of passive mixer, noise from higher order harmonics are also folded down which increased its noise contribution.

III. Implementation and Measruement Results

The proposed SDR receiver frontend RFIC is implemented in a 0.18 μm BiCMOS technology. The first stage LNA consumes

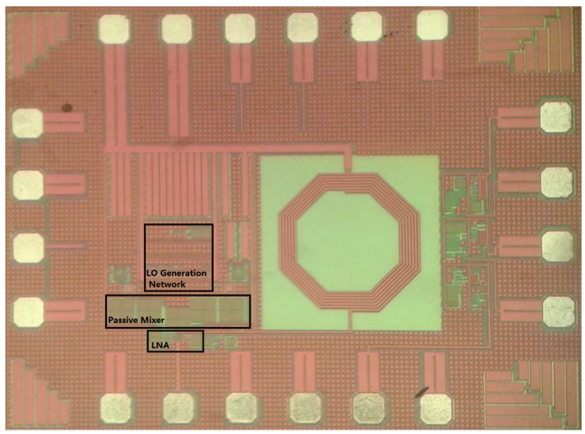

Fig. 3. Die photo of the proposed frontend.

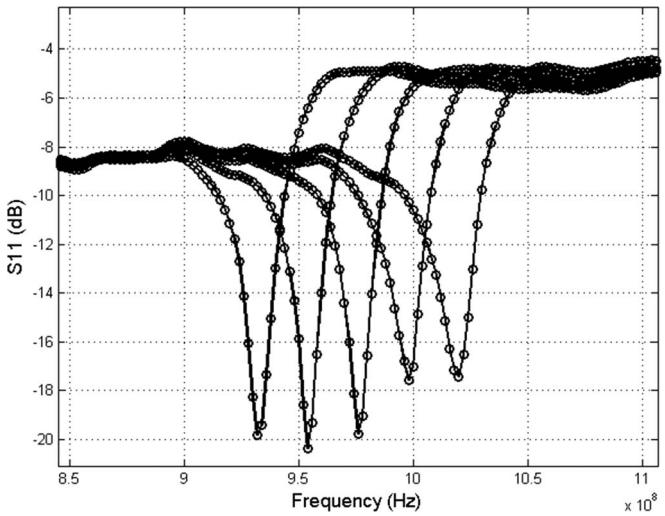

Fig. 4. Measured input S_{11} by tuning the LO frequency, the front end is only input matched at target band.

5.4 mW with a biasing current of 3 mA (g_m of 110 mS) to achieve the minimum NF. The multi-phase clock generation circuit using cascaded frequency dividers consumes 68.4 mW and the baseband amplifiers including output buffers consume 13 mW under a supply voltage of 1.8 V. The die photo is shown in Fig. 3. The total area excluding pads is approximately 0.44 mm^2 and the core area of the frontend is only 0.12 mm^2.

An output buffer was added at the LNA output (not shown in Fig. 1) in order to measure the S-parameter of the first stage alone. The measured S_{11} and S_{21} are shown in Figs. 4 and 5, respectively. The measured S11 shows unbalanced behavior between lower and upper sideband due to input parasitic including the DC inductors and wirebond inductance. The measured in-band (IB) and out-of-band (OB) IIP3 are -11 dBm and $+3$ dBm, respectively. The measured linearity performance is better than what can be achieved using a conventional LNA first receiver without feedback [6]. The measured total NF of the frontend is 4.6 dB which is better than the mixer first [5] reconfigurable designs. The measured performances of the proposed reconfigurable SDR receiver RFIC is summarized in Table I with comparisons to other published designs. The proposed reconfigurable frontend design achieved favorable noise and linearity performances with good out-of-band interferer tolerance.

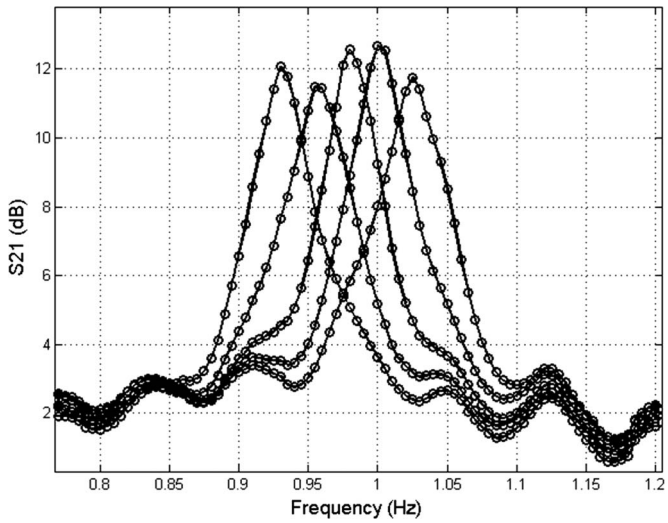

Fig. 5. Measured LNA gain S_{21} by tuning the LO frequency showing a 10 dB gain difference between in-band and out-of-band signals.

TABLE I
RECEIVER PERFORMANCE SUMMARY AND COMPARISON

	This Work	[4]	[5]	[6]
Architecture	LNA with capacitive feedback	LNA with shunt feedback	Mixer first	Current mode LNA
Selective Input Matching	Yes	Yes	No	No
Voltage Gain	40dB	38dB	25dB	23dB
Noise Figure	4.6dB	5.6dB	7.7dB	6.5dB
Operating Frequency	0.6-1.1GHz	0.7-2.7GHz	1.55-2.3GHz	1.0-5.2 GHz
IB IIP3	-11 dBm	-12.7 dBm	-	-
OB IIP3 *	+3 dBm	+1 dBm	+7 dBm	-1.5 dBm
Supply Voltage	1.8V	1.1V	2V	1.2V
Core Power **	5.4mW	15.4mW	10mW	13mW
Technology	180nm BiCMOS	40nm CMOS	180nm CMOS	130nm CMOS

IV. CONCLUSION

A reconfigurable RF frontend with tunable channel filtering and input matching at the LNA input is demonstrated in this letter. The proposed receiver front-end achieved improved blocker tolerance using only one down-conversion path and only one additional capacitor to form a capacitive feedback, resulting in a highly effective, yet quite simple reconfigurable SDR frontend architecture.

REFERENCES

[1] C. Andrews *et al.*, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.
[2] D. Murphy, "Noise in Large-Signal, Time-Varying RF CMOS Circuits: Theory & Design," Ph.D. Dissertation, Dept. Elect. Eng., Univ. of California, Los Angeles, CA, 2012.
[3] P. Rossi *et al.*, "A variable gain RF front-end based on a voltage-voltage feedback LNA for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 690–697, Mar. 2005.
[4] K. B. Ostman *et al.*, "Analysis and design of N-path filter offset tuning in a 0.7–2.7-GHz receiver front-end," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 1, pp. 234–243, Jan. 2015.
[5] N. Kim *et al.*, "A resistively degenerated wideband passive mixer with low noise figure and high IIP2," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 4, pp. 820–830, Apr. 2010.
[6] K. Jusung *et al.*, "Low-power, low-cost CMOS direct-conversion receiver front-end for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2090–2103, Sep. 2013.